LETTERS

Enhanced thermoelectric performance of rough silicon nanowires

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Approximately 90 per cent of the world's power is generated by heat engines that use fossil fuel combustion as a heat source and typically operate at 30–40 per cent efficiency, such that roughly 15 terawatts of heat is lost to the environment. Thermoelectric modules could potentially convert part of this low-grade waste heat to electricity. Their efficiency depends on the thermoelectric figure of merit ZT of their material components, which is a function of the Seebeck coefficient, electrical resistivity, thermal conductivity and absolute temperature. Over the past five decades it has been challenging to increase $ZT > 1$, since the parameters of ZT are generally interdependent[1]. While nanostructured thermoelectric materials can increase $ZT > 1$ (refs 2–4), the materials (Bi, Te, Pb, Sb, and Ag) and processes used are not often easy to scale to practically useful dimensions. Here we report the electrochemical synthesis of large-area, wafer-scale arrays of rough Si nanowires that are 20–300 nm in diameter. These nanowires have Seebeck coefficient and electrical resistivity values that are the same as doped bulk Si, but those with diameters of about 50 nm exhibit 100-fold reduction in thermal conductivity, yielding $ZT = 0.6$ at room temperature. For such nanowires, the lattice contribution to thermal conductivity approaches the amorphous limit for Si, which cannot be explained by current theories. Although bulk Si is a poor thermoelectric material, by greatly reducing thermal conductivity without much affecting the Seebeck coefficient and electrical resistivity, Si nanowire arrays show promise as high-performance, scalable thermoelectric materials.

The most widely used commercial thermoelectric material is bulk Bi_2Te_3 and its alloys with Sb, Se, and so on, which have $ZT = S^2T/\rho k \approx 1$, where S, ρ, k and T are the Seebeck coefficient, electrical resistivity, thermal conductivity and absolute temperature, respectively. It is difficult to scale bulk Bi_2Te_3 to large-scale energy conversion, but fabricating synthetic nanostructures for this purpose is even more difficult and expensive. Si, on the other hand, is the most abundant and widely used semiconductor, with a large industrial infrastructure for low-cost and high-yield processing. Bulk Si, however, has a high k ($\sim 150\ W\ m^{-1}\ K^{-1}$ at room temperature)[5], giving $ZT \approx 0.01$ at 300 K (ref. 6). The spectral distribution of phonons contributing to the k of Si at room temperature is quite broad. Because the rate of phonon–phonon Umklapp scattering scales as ω^2, where ω is the phonon frequency, low-frequency (or long-wavelength) acoustic phonons have long mean free paths and contribute significantly to k at high temperatures[7–10]. Thus, by rational incorporation of phonon-scattering elements at several length scales, the k of Si is expected to decrease dramatically. The ideal thermoelectric material is believed to be a phonon glass and an electronic crystal. Here, we show that by using roughened nanowires, we can reduce the thermal conductivity to $\sim 1.6\ W\ m^{-1}\ K^{-1}$, with the phonon contribution close to the amorphous limit, without significantly modifying the power factor S^2/ρ, such that $ZT \approx 1$ at room temperature. Further reduction of nanowire diameter is likely to increase ZT to >1.

Wafer-scale arrays of Si nanowires were synthesized by an aqueous electroless etching (EE) method[11–13]. The technique is based on the galvanic displacement of Si by $Ag^+ \rightarrow Ag^0$ reduction on the wafer surface. The reaction proceeds in an aqueous solution of $AgNO_3$ and HF acid. Briefly, Ag^+ reduces onto the Si wafer surface by injecting holes into the Si valence band and oxidizing the surrounding lattice, which is subsequently etched by HF. The initial reduction of Ag^+ forms Ag nanoparticles on the wafer surface, thus delimiting the spatial extent of the oxidation and etching process. Further reduction of Ag^+ occurs on the nanoparticles, not the Si wafer, which becomes the active cathode by electron transfer from the underlying wafer. Ag dentritic growth on the arrays can be washed off with deionized water after the synthesis. The arrays were washed in a concentrated nitric acid bath for at least one hour to remove all residual Ag from the nanowire surfaces. After the nitric acid bath, no Ag particles were observed during transmission electron microscopy (TEM) analysis and no Ag peaks appeared in the energy-dispersive X-ray spectra of the nanowires. Furthermore, the reaction proceeds at or near room temperature (295 K), so no diffusion of Ag atoms into a covalent solid lattice—such as Si—should be expected.

Nanowires synthesized by this approach were vertically aligned and consistent throughout batches, and across large areas up to wafer-scale. Figure 1a is a cross-sectional scanning electron microscope (SEM) image of one such array, and the inset shows a one-inch-square nanowire array. Key parameters of the reaction were identified using p-type ⟨100⟩-oriented, nominally 10–20 Ω cm, Si as the etch wafer. Both etching time and $AgNO_3$ concentration controlled nanowire length, roughly linearly, down to 5 μm at short immersion times (<10 min). At longer etching times, nanowire lengths were controllable up to 150 μm, while longer wires were too fragile to preserve the array. Wafers cut to ⟨100⟩, ⟨110⟩ and ⟨111⟩ orientations all yielded nanowire arrays etched normal to the wafer surface over most of the wafer area. Similar results were obtained for EE of both n- and p-type wafers with resistivities varying from 10 to $10^{-2}\ \Omega$ cm ($\sim 10^{14}$ to $10^{18}\ cm^{-3}$ dopant concentrations). Because thermoelectric modules consist of complementary p- and n-type materials wired in series, the generality and scalability of this synthesis are promising for fabrication of Si-based devices.

After etching, the fill factor of the nanowires was approximately 30% over the entire wafer surface. The nanowires varied from 20 to 300 nm in diameter with an average diameter of approximately 100 nm, as measured from TEM micrographs (Fig. 1b). The

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nanowires were single crystalline, as shown by the selected area electron diffraction pattern (top inset) and high-resolution TEM image of the Si lattice of an EE nanowire in Fig. 1c. In contrast to the smooth surfaces of typical vapour–liquid–solid (VLS)-grown, gold-catalysed Si nanowires (Fig. 1d)[14,15], those of the EE Si nanowires are much rougher. The mean roughness height of these nanowires varied from wire to wire, but was typically 1–5 nm with a roughness period of the order of several nanometres. This roughness may be attributed to randomness of the lateral oxidation and etching in the corrosive aqueous solution or slow HF etching and faceting of the lattice during synthesis.

The main advantage of using Si nanowires for thermoelectric applications lies in the large difference in mean free path lengths between electrons and phonons at room temperature: 110 nm for electrons in highly doped samples[16,17] and ~300 nm for phonons[10]. Consequently, incorporating structures with critical dimensions/spacings below 300 nm in Si should reduce the thermal conductivity without significantly affecting S^2/ρ. The thermal conductivity of these hierarchically structured Si nanowires was characterized using devices consisting of resistive coils supported on parallel, suspended SiN_X membranes[14,18]. This construction allows us to probe thermal transport in individual nanowires. The membranes are thermally connected through a bridging nanowire, with negligible leakage from heat transfer by means other than conduction through the wire. The thermal conductivity was extracted from the thermal conductance using the dimensions of the nanowire, as determined by SEM. To anchor the nanowire to the membranes and reduce thermal contact resistance, a Pt/C composite was deposited on both ends using a focused electron beam (Fig. 2a, also see Supplementary Information). The contact resistance at the interface between the nanowire and the pad is negligible relative to the nanowire thermal resistance. This condition was verified by measuring the thermal conductivity of a large nanowire (135 nm diameter) after two rounds of thermal anchoring with Pt/C pads. The second thermal anchoring doubled the contact area of the nanowire with the Pt/C pad and the SiN_X membrane, and the measured thermal conductivity of the wire remained unchanged. Hence, the nanowire thermal resistance dominates over that of the contacts (see Supplementary Fig. 2).

Figure 2b shows the measured thermal conductivity of both VLS and EE Si nanowires. It has been shown that the k of VLS Si nanowires is strongly diameter-dependent[14], which is attributed to boundary scattering of phonons. We found that EE Si nanowires exhibit a diameter dependence of k similar to that of VLS-grown wires. The magnitude of k, however, is five- to eightfold lower for EE nanowires of comparable diameters. Because the phonon spectrum is broad and Planck-like, k can be reduced by introducing scattering at additional length scales beyond the nanowire diameter[1–4,19]. In the case of the EE nanowires, the roughness at the nanowire surface behaves like secondary scattering phases. The roughness may contribute to higher rates of diffuse reflection or backscattering of phonons at

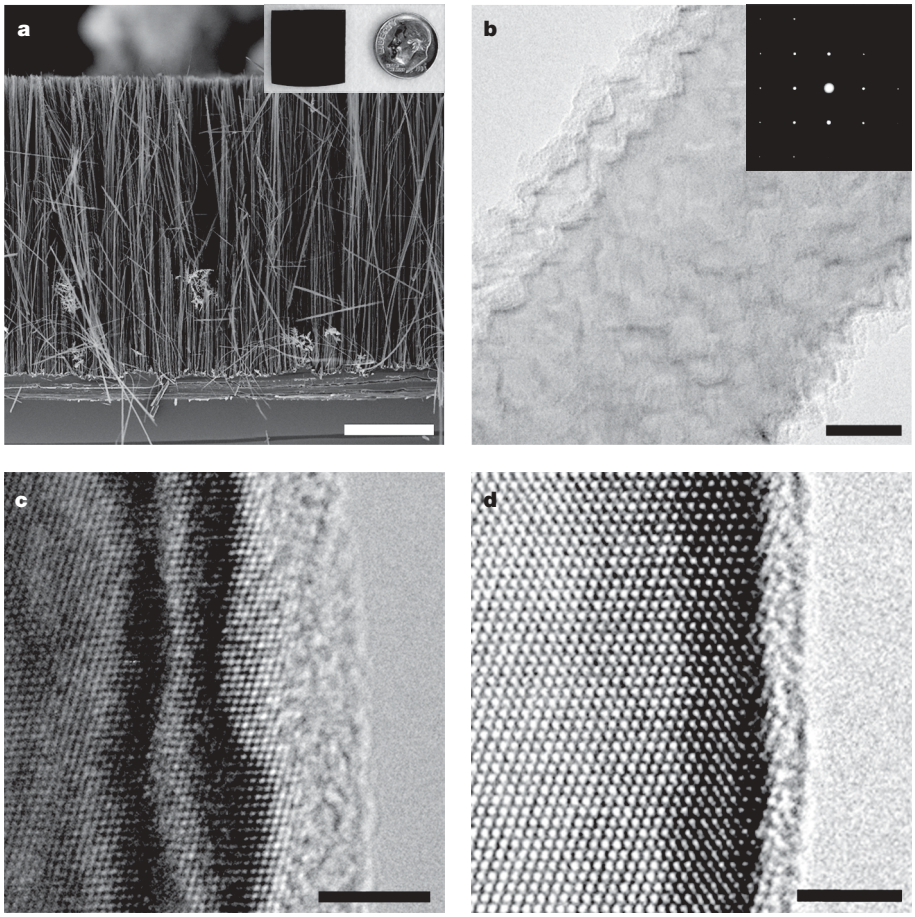

Figure 1 | Structural characterization of the rough silicon nanowires. **a**, Cross-sectional SEM of an EE Si nanowire array. Dendritic Ag growth can be seen within the array—a product of Ag^+ reduction onto the wafer during reaction. The Ag is etched in nitric acid after the synthesis, and elemental analysis confirms it is dissolved completely. Inset, an EE Si nanowire array Si wafer chip of the typical size used for the syntheses. Similar results are obtained on entire 4-inch wafers. The chip is dark and non-reflective owing to light scattering by, and absorbing into, the array. **b**, Bright-field TEM image of a segment of an EE Si nanowire. The roughness is clearly seen at the surface of the wire. The selected area electron diffraction pattern (inset) indicates that the wire is single crystalline all along its length. **c**, High-resolution TEM image of an EE Si nanowire. The roughness is evident at the interface between the crystalline Si core and the amorphous native oxide at the surface, and by undulations of the alternating light/dark thickness fringes near the edge. **d**, High-resolution TEM of a VLS-grown Si nanowire. Scale bars for **a**–**d** are 10 μm, 20 nm, 4 nm and 3 nm, respectively.

the interfaces. These processes have been predicted to affect the k values of Si nanowires, but not to the extent observed here[20,21]. The peak k of the EE nanowires is shifted to a much higher temperature than that of VLS nanowires, and both are significantly higher than that of bulk Si, which peaks at around 25 K (ref. 5). This shift suggests that the phonon mean free path is limited by boundary scattering as opposed to intrinsic Umklapp scattering.

While the above wires were etched from high-resistivity wafers, the peak ZT of semiconductor materials is predicted to occur at high dopant concentrations ($\sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$; ref. 22). To optimize the ZT of EE nanowires, lower resistivity nanowires were synthesized from $10^{-1}\,\Omega\,\mathrm{cm}$ B-doped p-Si ⟨111⟩ and $10^{-2}\,\Omega\,\mathrm{cm}$ As-doped n-Si ⟨100⟩ wafers by the standard method outlined above. Nanowires etched from the $10^{-2}\,\Omega\,\mathrm{cm}$ and less resistive wafers, however, did not produce devices with reproducible electrical contacts, probably owing to greater surface roughness, as observed in TEM analysis. Consequently, more optimally doped nanowires were obtained by post-growth gas-phase B doping of wires etched from $10^{-1}\,\Omega\,\mathrm{cm}$ wafers (see Supplementary Information). The resulting nanowires have an average $\rho = 3 \pm 1.4\,\mathrm{m}\Omega\,\mathrm{cm}$ (as compared to $\sim 10\,\Omega\,\mathrm{cm}$ for wires from low-doped wafers).

Figure 2c shows the k of small-diameter nanowires etched from 10, 10^{-1}, and $10^{-2}\,\Omega\,\mathrm{cm}$ wafers. The post-growth doped nanowire (52 nm diameter) etched from a $10^{-1}\,\Omega\,\mathrm{cm}$ wafer has a slightly lower k than the lower-doped wire of the same diameter. This small decrease in k may be attributed to higher rates of phonon-impurity scattering. Studies of doped and isotopically purified bulk Si have revealed a reduction of k as a result of impurity scattering[6,23,24]. Owing to the atomic nature of such defects, they are expected to predominantly scatter short-wavelength phonons. On the other hand, nanowires etched from a $10^{-2}\,\Omega\,\mathrm{cm}$ wafer have a much lower k than the other nanowires, probably as a result of the greater surface roughness.

In the case of the 52 nm nanowire, k is reduced to $1.6 \pm 0.13\,\mathrm{W\,m^{-1}\,K^{-1}}$ at room temperature. For comparison, the temperature-dependent k of amorphous bulk SiO_2 (data points used from http://users.mrl.uiuc.edu/cahill/tcdata/tcdata.html agree with measurement in ref. 25) is also plotted in Fig. 2c. As can be seen from the plot, k of these single-crystalline EE Si nanowires is comparable to that of insulating glass. Indeed, k of the 52 nm nanowire approaches the minimum k predicted and measured for Si: $\sim 1\,\mathrm{W\,m^{-1}\,K^{-1}}$ (ref. 26). The resistivity of a single nanowire of comparable diameter (48 nm) was measured (see Supplementary Information) and the electronic contribution to thermal conductivity (k_e) can be estimated from the Wiedemann–Franz law[16]. For measured $\rho = 1.7\,\mathrm{m}\Omega\,\mathrm{cm}$, $k_e = 0.4\,\mathrm{W\,m^{-1}\,K^{-1}}$, meaning that the lattice thermal conductivity ($k_l = k - k_e$) is $1.2\,\mathrm{W\,m^{-1}\,K^{-1}}$.

By assuming the mean free path due to boundary scattering $\ell_b = Fd$, where $F > 1$ is a multiplier that accounts for the specularity of phonon scattering at the nanowire surface and d is the nanowire diameter, a model based on Boltzmann transport theory was able to explain[27] the diameter dependence of thermal conductivity in VLS nanowires, as observed in ref. 14. Because the thermal conductivity of EE nanowires is lower and the surface is rougher than that of VLS ones, it is natural to assume $\ell_b = d$ ($F = 1$), which is the smallest mean free path due to boundary scattering. However, this still cannot explain why the phonon thermal conductivity approaches the amorphous limit for nanowires with diameters ~ 50 nm. In fact, theories that consider phonon backscattering, as recently proposed by ref. 21, cannot explain our observations either. The thermal conductivity in amorphous non-metals[26] can be well explained by

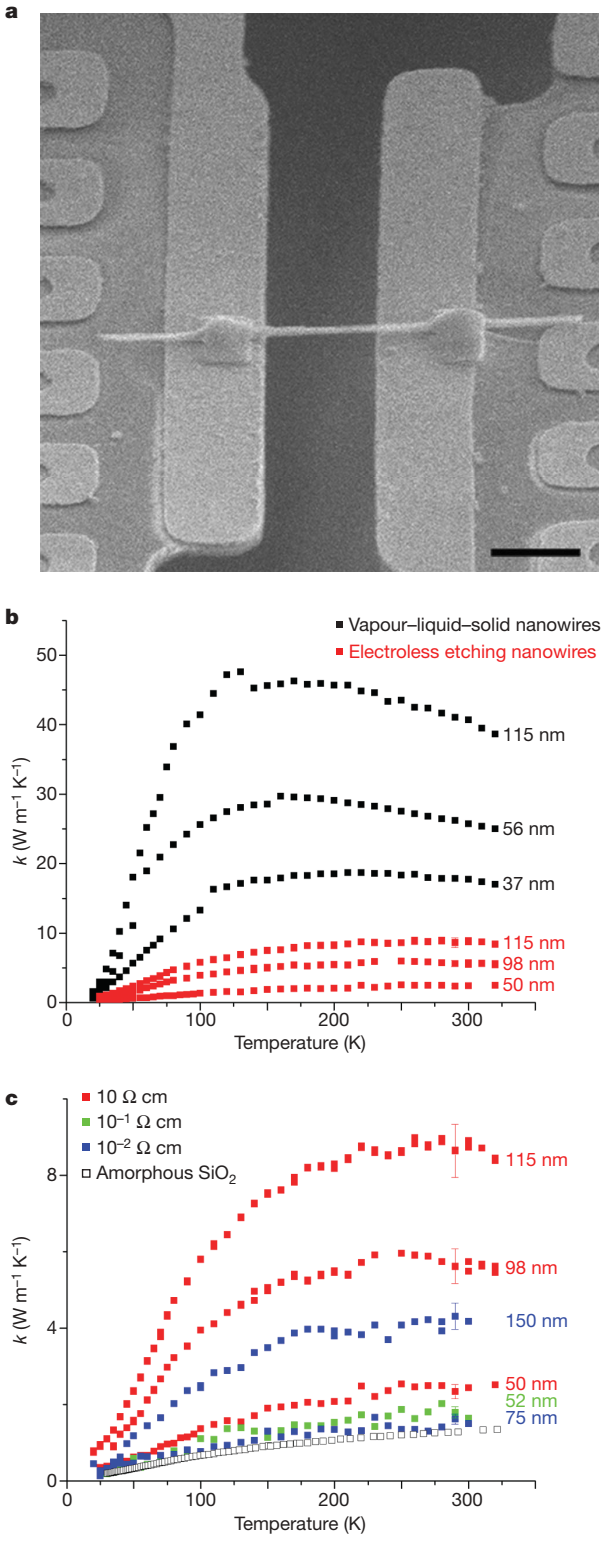

Figure 2 | Thermal conductivity of the rough silicon nanowires. **a**, An SEM image of a Pt-bonded EE Si nanowire (taken at 52° tilt angle). The Pt thin film loops near both ends of the bridging wire are part of the resistive heating and sensing coils on opposite suspended membranes. Scale bar, 2 μm. **b**, The temperature-dependent k of VLS (black squares; reproduced from ref. 14) and EE nanowires (red squares). The peak k of the VLS nanowires is 175–200 K, while that of the EE nanowires is above 250 K. The data in this graph are from EE nanowires synthesized from low-doped wafers. **c**, Temperature-dependent k of EE Si nanowires etched from wafers of different resistivities: $10\,\Omega\,\mathrm{cm}$ (red squares), $10^{-1}\,\Omega\,\mathrm{cm}$ (green squares; arrays doped post-synthesis to $10^{-3}\,\Omega\,\mathrm{cm}$), and $10^{-2}\,\Omega\,\mathrm{cm}$ (blue squares). For the purpose of comparison, the k of bulk amorphous silica is plotted with open squares. The smaller highly doped EE Si nanowires have a k approaching that of insulating glass, suggesting an extremely short phonon mean free path. Error bars are shown near room temperature, and should decrease with temperature. See Supplementary Information for k measurement calibration and error determination.

assuming that the phonon mean free path $\ell = \lambda/2$, where λ is the phonon wavelength, which invokes a Debye-like short-range coherence in an atomically disordered lattice. However, there seems no justifiable reason to make this assumption for the single-crystal EE Si nanowires, because their diameters are about 100-fold larger than the lattice constant. To the best of our knowledge, there is currently no theory that can explain why a single-crystalline Si nanowire that is ~50 nm in diameter should behave like a phonon glass. On the basis of the difference between VLS and EE nanowires, we suspect that the roughness plays a strong role in screening a broad spectrum of phonons, fundamentally altering phonon transmission through these confined structures. The exact mechanism, however, remains unknown.

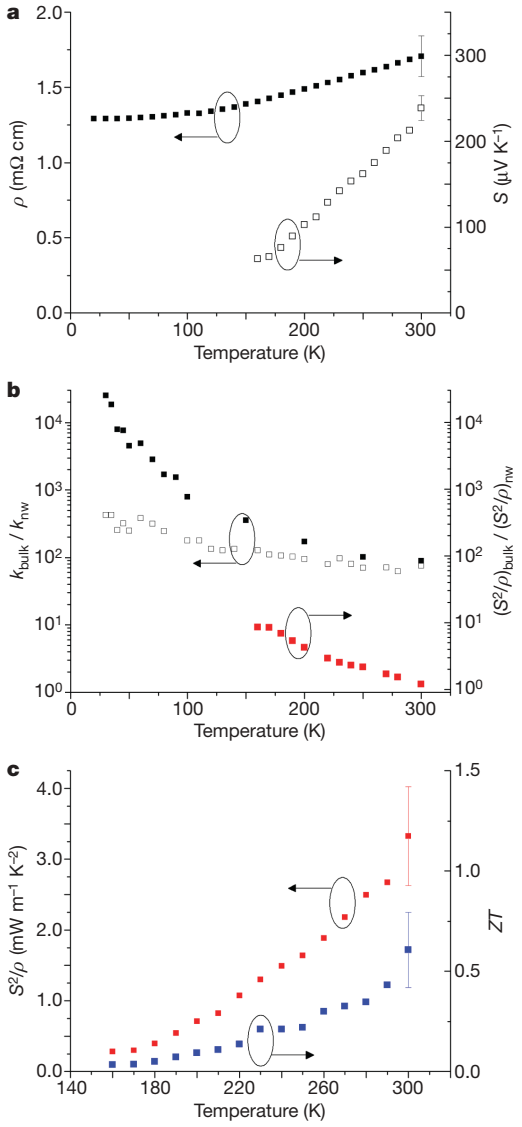

Figure 3 | Thermoelectric properties and *ZT* calculation for the rough silicon nanowire. **a**, S (open squares) and ρ (solid squares) of the highly doped EE 48 nm nanowire. See Supplementary Information for error analysis. **b**, Ratio of intrinsic bulk Si k (ref. 5) to that of a highly doped EE Si nanowire 50 nm in diameter. k_{bulk}:k_{nw} increases dramatically with decreasing temperature, from 100 at 300 K to 25,000 at 25 K (solid squares). As compared to highly doped bulk Si (1.7×10^{19} cm^{-3} As-doped, data adapted from ref. 6), k_{bulk}:k_{nw} increases from 75 at 300 K to 425 at 30 K (open squares). Red squares show the ratio of the power factor of optimally doped bulk Si relative to the nanowire power factor as a function of temperature. **c**, Single nanowire power factor (red squares) of the nanowire and calculated ZT (blue squares) using the measured k of the 52 nm nanowire in Fig. 2c. By propagation of uncertainty from the ρ and S measurements, the error bars are 21% for the power factor and 31% for ZT (assuming negligible temperature uncertainty, which seems valid given that the measurements are stable to better than ±100 mK).

To calculate the nanowire ZT, ρ and S measurements were carried out on individual highly doped nanowires. One such measurement on a 48 nm diameter wire is shown in Fig. 3a. Nanowires were measured in a horizontal geometry on 200 nm SiN_X films on Si substrates with a microfabricated heating element, and 2- and 4-point probe electrodes (see Supplementary Fig. 3). The power factor was calculated as $S^2/\rho = 3.3 \times 10^{-3}$ W m^{-1} K^{-2} for the nanowire at 300 K. The ratio of the power factor of optimally doped bulk Si to that of the EE Si nanowire as a function of temperature is plotted in Fig. 3b (with bulk values taken from ref. 6). The nanowire power factor decreases gradually relative to bulk with decreasing temperature, possibly due to a longer electron mean free path. On the other hand, as temperature decreases, the disparity between k of the nanowire and bulk grows. At low temperatures, long-wavelength phonon modes, which contribute strongly to thermal transport in bulk, are efficiently scattered in the roughened nanowires.

Figure 3b charts the ratio of k_{bulk}:k_{nw} for the 52 nm highly doped EE Si nanowire as a function of temperature. Whereas the k_{nw} is two orders of magnitude lower than k_{bulk} at room temperature, this ratio reaches more than four orders of magnitude at low temperature. Also shown is k_{bulk}:k_{nw} for highly doped bulk Si, for which k_{bulk}:k_{nw} is greatly reduced at low temperature. The large disparity persists unchanged, however, near room temperature. As a result, the degradation of the nanowire power factor with decreasing temperature is offset by the significant decrease in k, resulting in a relatively constant ZT enhancement factor for the EE Si nanowire.

ρ and S of the 48 nm nanowire were used for the ZT calculation because the diameter is close to that of the 52 nm wire for which k has been measured. The nanowire ZT is highest near room temperature at 0.6 (Fig. 3c). As compared to optimally doped bulk Si (~1×10^{19} cm^{-3}), the ZT of the EE nanowire is nearly two orders of magnitude greater throughout the temperature range measured[6]. The large increase in ZT is due to the significant decrease of k as compared to bulk while maintaining a high power factor. The hierarchical structuring of the EE Si nanowires allows selective scattering of phonons by dopants, nanoscale surface roughness, and dimensional confinement, while leaving electronic transport largely unaffected.

In conclusion, we have shown that it is possible to achieve $ZT = 0.6$ at room temperature in rough Si nanowires of ~50 nm diameter that were processed by a wafer-scale manufacturing technique. With optimized doping, diameter reduction, and roughness control, the ZT is likely to rise even higher. This ZT enhancement can be attributed to efficient scattering throughout the phonon spectrum by the introduction of nanostructures at different length scales (diameter, roughness and point defects). The significant reduction in thermal conductivity observed in this study may be a result of changes in the fundamental physics of heat transport in these quasi-one-dimensional materials. By achieving broadband impedance of phonon transport, we have demonstrated that the EE Si nanowire system is capable of approaching the limits of minimum lattice thermal conductivity in Si. Modules with the performance reported here, and manufactured from such a ubiquitous material as Si, may find wide-ranging applications in waste heat salvaging, power generation, and solid-state refrigeration. Moreover, the phonon scattering techniques developed in this study could significantly augment ZT even further in other materials to produce highly efficient solid-state thermoelectric devices.

METHODS SUMMARY

Nanowires were typically etched from B-doped Si wafers of different resistivities in aqueous solutions of 0.02 M $AgNO_3$ and 5 M HF for several hours. Excess Ag was removed in a nitric acid bath for at least one hour. Highly doped nanowires were achieved by annealing arrays at 850 °C for one hour in BCl_3 vapour. The

structure and microstructure of nanowire arrays and individual nanowires were characterized using SEM and TEM.

For thermal conductivity measurements, nanowires were either drop-cast onto the microfabricated devices from dispersions in isopropanol, or placed directly on the devices by micromanipulation with narrow tungsten probe tips (GGB Industries) mounted on a scanning stage (Marzhauser SM 3.25). The thermal conductivity of individual nanowires was measured by the previously described method[14,18].

The electrical conductivity and Seebeck coefficient of EE Si nanowires were measured by drop-casting isopropanol dispersions of nanowires onto Si wafer substrates coated with a 200-nm-thick silicon nitride film. Metal contact lines and a heating coil were fabricated on the same wafers using standard optical lithography (see Supplementary Fig. 3). 2- and 4-point I–V measurements, and dimensions from SEM images, were used to determine ρ for individual nanowires. S of single nanowires was measured by applying a current to the heating coil and measuring the temperature between the two inner 4-point probe contacts. 4-point measurements of both contact lines, and measured R versus T calibration curves were used to calculate the ΔT between them. S was calculated by $S = \Delta V/\Delta T$.

Full Methods and any associated references are available in the online version of the paper at www.nature.com/nature.

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1. Majumdar, A. Thermoelectricity in semiconductor nanostructures. *Science* **303,** 777–778 (2004).
2. Hsu, K. F. *et al.* Cubic $AgPb_mSbTe_{2+m}$: bulk thermoelectric materials with high figure of merit. *Science* **303,** 818–821 (2004).
3. Harman, T. C., Taylor, P. J., Walsh, M. P. & LaForge, B. E. Quantum dot superlattice thermoelectric materials and devices. *Science* **297,** 2229–2232 (2002).
4. Venkatasubramanian, R., Siivola, E., Colpitts, T. & O'Quinn, B. Thin-film thermoelectric devices with high room-temperature figures of merit. *Nature* **413,** 597–602 (2001).
5. Touloukian, Y. S., Powell, R. W., Ho, C. Y. & Klemens, P. G. (eds) *Thermal Conductivity: Metallic Elements and Alloys, Thermophysical Properties of Matter* Vol. 1, 339 (IFI/Plenum, New York, 1970).
6. Weber, L. & Gmelin, E. Transport properties of silicon. *Appl. Phys. A* **53,** 136–140 (1991).
7. Nolas, G. S., Sharp, J. & Goldsmid, H. J. in *Thermoelectrics: Basic Principles and New Materials Development* (eds Nolas, G. S., Sharp, J. & Goldsmid, H. J.) Ch. 3 (Springer, Berlin, 2001).
8. Asheghi, M., Leung, Y. K., Wong, S. S. & Goodson, K. E. Phonon-boundary scattering in thin silicon layers. *Appl. Phys. Lett.* **71,** 1798–1800 (1997).
9. Asheghi, M., Touzelbaev, M. N., Goodson, K. E., Leung, Y. K. & Wong, S. S. Temperature-dependent thermal conductivity of single-crystal silicon layers in SOI substrates. *J. Heat Transf.* **120,** 30–36 (1998).
10. Ju, Y. S. & Goodson, K. E. Phonon scattering in silicon films with thickness of order 100 nm. *Appl. Phys. Lett.* **74,** 3005–3007 (1999).
11. Peng, K. Q., Yan, Y. J., Gao, S. P. & Zhu, J. Synthesis of large-area silicon nanowire arrays via self-assembling nanochemistry. *Adv. Mater.* **14,** 1164–1167 (2002).
12. Peng, K., Yan, Y., Gao, S. & Zhu, J. Dendrite-assisted growth of silicon nanowires in electroless metal deposition. *Adv. Funct. Mater.* **13,** 127–132 (2003).
13. Peng, K. *et al.* Uniform, axial-orientation alignment of one-dimensional single-crystal silicon nanostructure arrays. *Angew. Chem. Intl Edn.* **44,** 2737–2742 (2005).
14. Li, D. *et al.* Thermal conductivity of individual silicon nanowires. *Appl. Phys. Lett.* **83,** 2934–2936 (2003).
15. Hochbaum, A. I., Fan, R., He, R. & Yang, P. Controlled growth of Si nanowire arrays for device integration. *Nano Lett.* **5,** 457–460 (2005).
16. Ashcroft, N. W. & Mermin, N. D. *Solid State Physics* Chs 1, 2 and 13 (Saunders College Publishing, Fort Worth, 1976).
17. Sze, S. M. *Physics of Semiconductor Devices* Ch. 1 (John Wiley & Sons, New York, 1981).
18. Shi, L. *et al.* Measuring thermal and thermoelectric properties of one-dimensional nanostructures using a microfabricated device. *J. Heat Transf.* **125,** 881–888 (2003).
19. Kim, W. *et al.* Thermal conductivity reduction and thermoelectric figure of merit increase by embedding nanoparticles in crystalline semiconductors. *Phys. Rev. Lett.* **96,** 045901 (2006).
20. Zou, J. & Balandin, A. Phonon heat conduction in a semiconductor nanowire. *J. Appl. Phys.* **89,** 2932–2938 (2001).
21. Saha, S., Shi, L. & Prasher, R. Monte Carlo simulation of phonon backscattering in a nanowire. *Proc. ASME Int. Mech. Eng. Congr. Exp. (5–10 November 2006)* art. no. 15668 1–5 (ASME, Chicago, 2006).
22. Rowe, D. M. (ed.) *CRC Handbook of Thermoelectrics* Ch. 5 (CRC Press, Boca Raton, 1995).
23. Brinson, M. E. & Dunstan, W. Thermal conductivity and thermoelectric power of heavily doped n-type silicon. *J. Phys. C* **3,** 483–491 (1970).
24. Ruf, T. *et al.* Thermal conductivity of isotopically enriched silicon. *Solid State Commun.* **115,** 243–247 (2000).
25. Cahill, D. G. & Pohl, R. O. Thermal conductivity of amorphous solids above the plateau. *Phys. Rev. B* **35,** 4067–4073 (1987).
26. Cahill, D. G., Watson, S. K. & Pohl, R. O. Lower limit to the thermal conductivity of disordered crystals. *Phys. Rev. B* **46,** 6131–6140 (1992).
27. Mingo, N., Yang, L., Li, D. & Majumdar, A. Predicting the thermal conductivity of Si and Ge nanowires. *Nano Lett.* **3,** 1713–1716 (2003).

Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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METHODS

Nanowire synthesis. The standard nanowire synthesis was conducted on B-doped p-type (100) Si wafers. Wafer chips, typically 1 inch × 1 inch or larger, were sonicated in acetone and 2-propanol, and then put in a Teflon-lined autoclave in aqueous solution of 0.02 M $AgNO_3$ and 5 M HF. The autoclave was sealed and placed in an oven at 50 °C for one hour. For 150-μm-long nanowires, wafer chips were prepared in the same fashion, and placed in the autoclave with 0.04 M $AgNO_3$ and 5 M HF for four hours. Alternatively, similar results were obtained using the same reactant concentrations with chips in open polyethylene beakers at room temperature. Nanowires were also etched from entire Si wafers. Wafers were cleaned and placed in a Teflon dish with an identical etching solution and the synthesis ran at room temperature. The wafers etched in these conditions produced wires similar to those etched in the autoclave but <50 μm in length. The same reaction conditions were used on wafers of all orientations, dopant type and concentration. Small regions on all samples had nanowires etched at an angle to normal.

Wires doped for ZT determination were etched from 0.1 Ω cm B-doped p-Si (111) wafers under the standard reaction conditions. After synthesis, the intact arrays were annealed with BCl_3 vapour and 10% H_2 balance Ar at 850 °C (1:50 standard cubic centimetres per minute BCl_3:H_2/Ar) for one hour.

Nanowire characterization. Cross-sectional samples were prepared by cleaving the EE Si nanowire substrate and viewing normal to the cleaved surface. SEM images were obtained using a JEOL JSM-6340F field emission SEM and using the electron beam of a FEI Strata 235 Dual Beam Focused Ion Beam (FIB) microscope. TEM and high-resolution TEM images were collected with a Phillips CM200/FEG (field-emission gun) microscope at 200 kV.

Thermal anchoring of nanowires. EE Si nanowires were bonded to both suspended SiN_X membranes using a FEI Strata 235 Dual Beam FIB. A focused electron beam (5 kV, spot size 3) was used to deposit Pt selectively on both ends of the bridging nanowire. The incident beam causes secondary electron emission from the underlying material's surface, locally decomposing a metal-organic Pt precursor. Care was taken not to expose the sample to electron irradiation immediately following deposition, but some deposition always occurs within a 1–2 μm radius of the exposed region (see Supplementary Information).

Single nanowire resistivity and Seebeck coefficient measurement. Devices for ρ and S measurements were fabricated using standard photolithography and lift-off techniques. The nanowires were sonicated off the substrate in clean-room grade isopropyl alcohol and drop-cast on a 4-inch silicon wafer pre-coated with 200 nm silicon nitride. About 3,000 devices (see Supplementary Fig. 3a) were patterned on the whole wafer using a wafer stepper (GCA 6200). After developing the 1.1-μm-thick I-line photoresist (OCG OiR 897-10i) using OPD 4262 developer, the native oxide of the nanowires was removed by a HF dip (10:1 buffered, ~15 s) followed by deionized water rinse (~15 s) and nitrogen drying. The wafer was immediately loaded into a high-vacuum chamber to deposit ~100 nm Pt as the contact metal by sputtering (Edwards Auto 306) with the vacuum level better than 5×10^{-6} torr. The wafer was then soaked in acetone for ~2 h for lift-off. No further annealing step was necessary for getting ohmic contacts. With the proper number density of nanowires on the wafer, devices with single nanowires bridging two or four electrodes are found quite frequently.

Electrical measurements on such devices were made in a home-built probe station at room temperature or in a cryogenic chamber at temperatures ranging from 20 to 300 K. For ρ measurement, I–V curves of nanowires were recorded by a source-meter (Keithley 6430) and the resistance R was extracted by using $R = \mathrm{d}V/\mathrm{d}I$. Typical I–V curves measured at 20 and 300 K are shown in Supplementary Fig. 3b. For Si nanowire doped to the ~1 mΩ cm regime, the contact between Si and Pt is ohmic, and the contact resistance was found to be negligible after comparing the 2- and 4-point resistance measurements on some nanowires. ρ is calculated by using $\rho = RA/L$, where A is the cross-sectional area and L is the length of nanowires, which were determined by SEM after electrical characterization.

To measure S, a direct current I generated by the source-meter was applied on the Pt heater, which was ~12 μm away from the nanowire, resulting in a temperature gradient along the nanowire. The Seebeck voltage (ΔV_S) was measured by a multimeter (Agilent 34401a) with respect to the total heating power $P = VI$, where V is the voltage across the heater (see Supplementary Fig. 3c). The temperature difference ΔT corresponding to such ΔV_S was measured between the two central Pt/Si contacts (see Supplementary Information).