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Carbon nanotube arrays on silicon substrates and their possible application

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Abstract

A method to grow regular arrays of oriented carbon nanotubes on silicon substrates is presented. It has been found that porous silicon is an ideal substrate for growing self-oriented carbon nanotubes on large surfaces. The growth mechanism of nanotube arrays has been discussed. The potential applications of carbon nanotube arrays in flat panel display and in synthesizing of other semiconducting nanorods on silicon substrates through the carbon nanotube-confined reaction have also been studied. © 2000 Elsevier Science B.V. All rights reserved.

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1. Introduction

Growing organized carbon nanotubes on large-scale surfaces is challenging but critical to obtain scaled-up functional devices. Examples include scanning probes and sensors [1–5], field emitters [6–11], and nano-electronics [12]. Significant effort is required to grow nanotubes in a controlled fashion so that little or no post-growth manipulation or assembly is needed to build useful structures. This work reports progress in synthesizing large-scale regular arrays of carbon nanotubes that are self-oriented on silicon substrates.

The nanotubes are up to hundreds of microns long and remarkably, self-aligned normal to the substrate during growth in chemical vapor deposition. We find that porous silicon is an ideal substrate for growing self-oriented nanotubes on large surfaces. The amazing ability of nanotubes to grow perpendicular to the substrate surface originates from high dense nanoscale catalysts formed on porous silicon surface, catalyst-surface interaction, and van der Waals interaction between nanotubes. The self-oriented nanotube arrays should have a wide range of scientific and technological applications. Immediately, we find that they are superior field emission arrays. Furthermore, the nanotube arrays can be used as the template to synthesize other semiconductor nanowires on silicon

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substrate via a carbon nanotube-confined reaction [13]. These devices are directly synthesized and their scale-up will be entirely compatible with the existing processes of semiconductor technology.

We have explored both porous silicon and plain silicon wafers as supporting substrates for nanotube growth. For porous silicon, samples were obtained by electrochemical etching of heavily phosphor-doped n^+ -type Si (100) wafers (2 in in diameter, resistivity 0.008–0.018 Ω cm). Etching was carried out in a Teflon cell using a Pt cathode for 5 min under backside illumination with a halogen lamp. The etching solution contained one part hydrogen fluoride (50% aqueous solution) and one part ethanol, and the anodization current density was kept constant at 10 mA/cm². Under these conditions, the etched silicon has a thin nanoporous layer (with pore diameters of \sim 3 nm) on top of a macroporous layer (with submicrometer pores) [14,15]. For plain silicon substrates, they were purchased and used as is, without cleaning or removing the native oxide layer. All substrates were patterned with Fe films (5 nm thick) by electron beam evaporation through shadow masks, containing squared openings with side lengths of 10–250 μ m at pitch distances of 50–200 μ m. The substrates were then annealed in air at 300°C overnight. To synthesize carbon nanotube arrays, the substrates were placed in a cylindrical quartz boat sealed at one end and then inserted into the center of a 2 in quartz tube reactor housed in a tube furnace. The furnace was heated to 700°C in flowing Ar. Ethylene was then flown at 1000 sccm for 15–60 min, after which the furnace was cooled to room temperature.

Using a scanning electron microscope (SEM), we observed that three-dimensional regular arrays of nanotubes blocks or towers were formed on top of the patterned iron squares on the substrates (Fig. 1). Several features of the nanotube structures are apparent. Each nanotube block exhibits very sharp edges and corners in low-magnification SEM images. The width of the blocks is the same as that of the iron patterns.

Transmission electron microscopy (TEM) is used to further characterize the synthesized nanotubes. Several nanotube blocks were ultrasonicated in 1,2-dichloroethane and a few drops of the suspension were placed onto a TEM grid. TEM investigation showed that the material consisted of pure multi-walled nanotubes. Measurements on more than

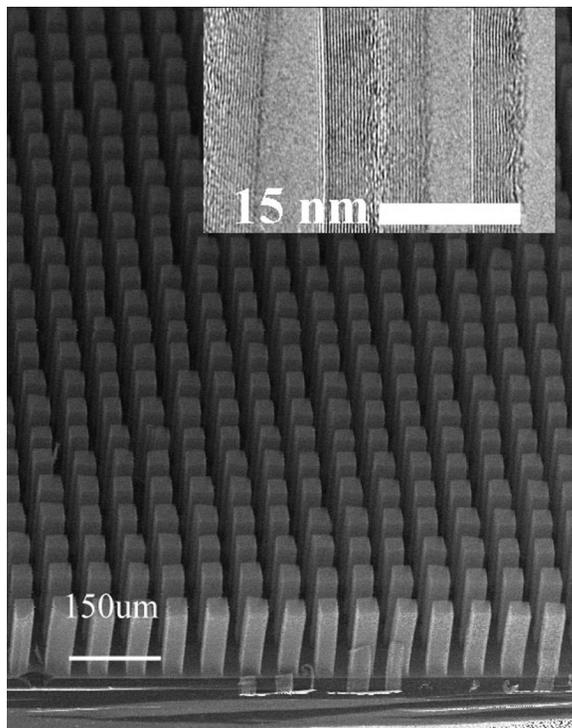


Fig. 1. Carbon nanotube arrays grown on n^+ -type porous silicon substrate.

100 nanotubes have diameters of 16 nm. TEM images show that our nanotubes contain a low defect density in some sections of their lengths (Fig. 1 inset). Even after ultrasonication, we still observe many aligned multi-walled nanotube bundles together with individual nanotubes that are separated from the bundles. This clearly indicates that the nanotubes within each block are relatively dense and form a giant bundle by van der Waals interaction.

We have also grown regular arrays of oriented nanotubes blocks on plain silicon (100) substrate (boron-doped p-type wafers, resistivity 5–10 Ω cm). The overall features of the nanotubes are similar to those grown on porous silicon. However, in contrast to porous silicon, we often find nanotube tower with high aspect ration falling onto the surface (Fig. 2) and some iron catalyst particles on the top of the nanotube block. This indicates weaker interactions at the interfaces between the nanotubes and the flat silicon surface. Another important difference is that the nanotubes appear to be less well aligned on plain

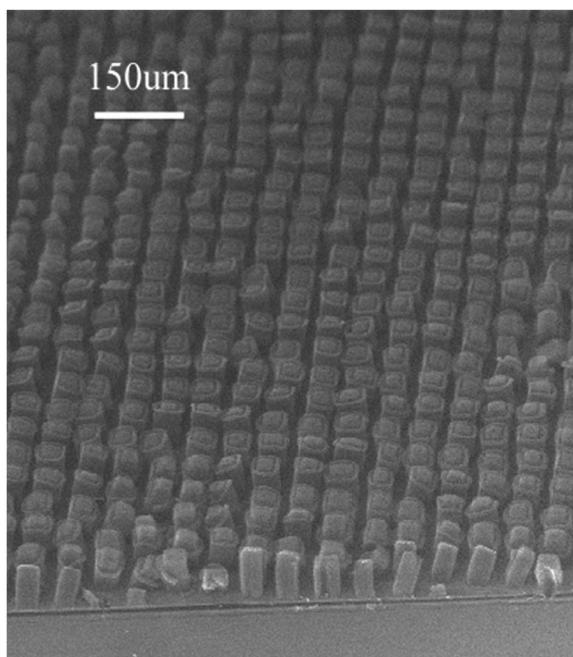


Fig. 2. Carbon nanotube arrays grown on p-type plain silicon substrate.

silicon substrates than on the porous silicon. In addition, TEM studies find that the nanotubes synthesized on plain silicon substrate have large diameters and tend to have a higher defect density than those on porous silicon. Nevertheless, the extreme simplicity of using plain silicon substrates for growing-oriented nanotube arrays on large wafers is attractive and will be further pursued.

We have observed that self-oriented nanotubes can be synthesized on both porous silicon and plain silicon substrates. Therefore, the nano- and micro-pores in the porous silicon substrates are not responsible for orienting nanotubes. However, we find that porous silicon substrates have several important advantages over plain silicon substrates. First, we have carried out several growth experiments that contain both porous silicon and plain silicon substrates at the same time. We clearly observed that the nanotubes grow at a rate that is about 50% faster on porous silicon than on silicon. This is rationalized by the fact that the porous silicon structure is permeable to the ethylene molecules so that carbon feedstock reaches the catalyst at a higher rate than on plain silicon substrate.

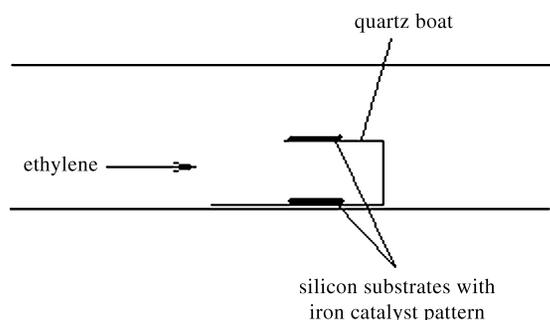


Fig. 3. Schematic diagram of the setup testing the influence of local environment.

Secondly, the nanoporous silicon layer acts as an excellent catalyst support. During the 300°C annealing step, iron oxide nanoparticles form with a narrow size distribution due to their strong interaction with the higher porous support. The strong interaction also prevents catalyst particles from sintering at elevated temperatures.

After physically removing nanotube blocks on several samples and heating the substrates in air to 700°C, the resulted substrates are still catalytically active for growing-oriented nanotube array. This result suggests that the base-growth mode dominates in our system. That is, catalyst particles interact strongly with the substrate and remain pinned during growth. A nanotube grows off each of the densely packed catalyst particles and extends to open space along the direction normal to the substrate. As the nanotubes lengthen, they interact with each other by van der Waals forces what let them to grow in one direction.

We also find that local environment above the silicon substrate plays another important role in nanotube arrays growth. We broke a porous silicon substrate into two pieces, then placed them inside and outside of a one-end sealed quartz boat, respectively (Fig. 3). After growth, the quality of the carbon nanotube array on the inside substrate was much better than that on the outside substrate. The main difference of growth condition between two substrates should be local flow rate and flow pattern of the reaction gases caused by different geometry around the substrates. It suggests that the local environment is also critical for catalytical growth of carbon nanotubes. However, the mechanism should be further studied.

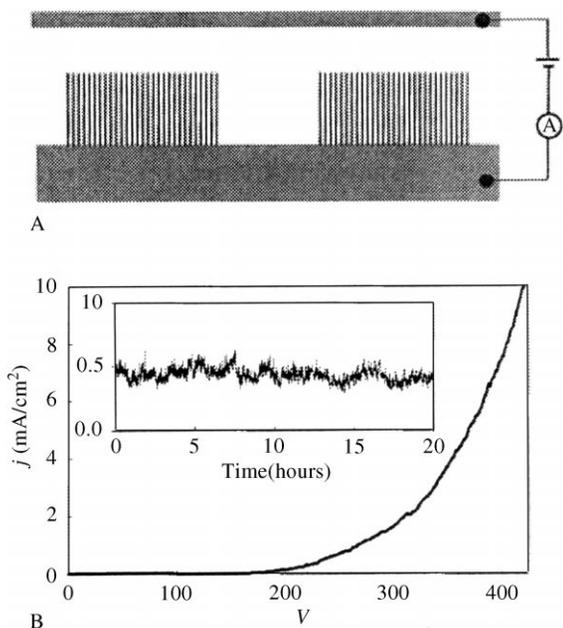
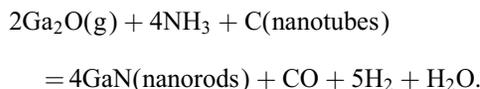


Fig. 4. Self-oriented nanotube arrays as electron field emitter arrays.

Carbon nanotubes have been identified as promising candidates for field emitters in applications such as flat panel displays. However, it remains unclear how to scale up these novel devices. This problem originates from the lack of strategies in scaling up nanotube growth and large-scale nanotube assembly and patterning. Using the synthesized self-oriented nanotube arrays without further sample processing, we have studied their properties as electron field emission arrays. The field emission experimental set-up is shown in (Fig. 4). The cathode consists of a n^+ -type porous silicon substrate with four $250 \times 250 \mu\text{m}$ nanotube locks. The height of the blocks is $130 \mu\text{m}$. An aluminum-coated silicon substrate serves as the anode and is kept as $200 \mu\text{m}$ away from the sample by a mica spacer containing a hole in the center. J - V characteristics were taken in a vacuum chamber at 3×10^{-7} Torr and were highly reproducible over repeated voltage scans. All samples tested exhibit low operating voltages and high current stability. With ~ 15 samples, we find that to reach current densities of 1 mA/cm^2 and 10 mA/cm^2 , the electric fields (calculated by using

the distance from the anode to the top of nanotube blocks) required are 2.7–3.3 and 4.8–6.1 V/m, respectively. Emission current was stable over a test period of 20 h at a current density of $\sim 0.5 \text{ mA/cm}^2$ (Fig. 4 inset). Their performances are comparable to the best field emission samples previously constructed by processing arc-discharge multiwalled or singlewalled nanotubes. Notably, our approach to these useful devices is via direct chemical synthesis of massive arrays of oriented nanotubes on macroscopic substrates.

Carbon nanotubes have been used as a template to fabricate other semiconducting nanowires, which are also of potential uses in both mesoscopic research and the development of nanodevices. In a previous work, we have synthesized GaN nanorods through a carbon nanotube-confined reaction [13]. There is no doubt that the method used there can also be used to convert carbon nanotube arrays on silicon substrate into GaN nanorod arrays on silicon substrate. An alumina boat containing a 4 : 1 molar mixture of Ga and Ga_2O_3 was placed in a horizontal quartz tube (Fig. 5a), through which Ar gas was flowing at 400 sccm. A silicon substrate with carbon nanotube arrays was placed nearby the mixture and downstream. The quartz tube was heated to 900°C , then Ar gas was switched to ammonia gas. It can be expected that ammonia and Ga_2O gas from reaction of Ga and Ga_2O_3 would flow over the carbon nanotube arrays and reacted with ammonia there:



The temperature was held to 900°C for 1 h and cooled down to room temperature with Ar flowing. It was found that the carbon nanotube array on silicon substrate had changed its colour from black to light yellow. SEM image shows that the carbon nanotubes had been changed to nanorods (Fig. 5b). EDAX spectrum shows that compositions of the nanorods are gallium and nitrogen. TEM images confirmed that the products were crystal GaN nanorods (Fig. 5b inset). No GaN nanorods were found in the areas between the carbon nanotube blocks on silicon substrate. It suggests that the GaN nanorods standing on silicon substrate were grown through the carbon nanotube-confined reaction. It can be speculated that

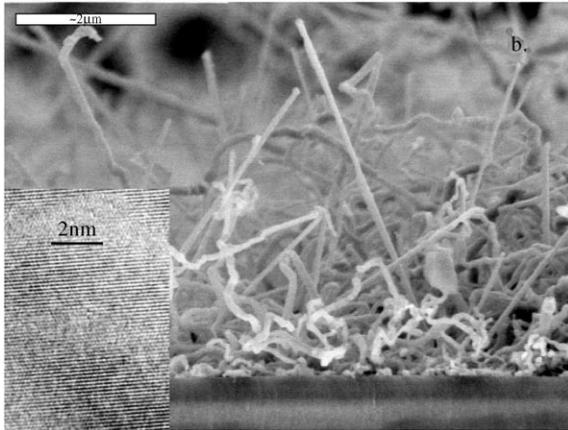
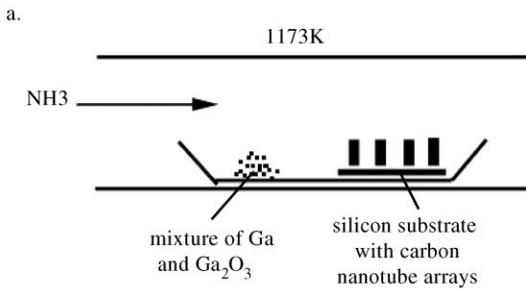


Fig. 5. GaN nanorod arrays grown on porous silicon substrate by carbon nanotubes-confined reaction. (a) Setup of experiments; (b) SEM and TEM images of standing GaN nanorods on substrate.

many kinds of semiconducting nanorods on silicon substrates can be made through this method.

We have synthesized regular arrays of oriented carbon nanotubes with high uniformity on silicon

substrates. The growth mechanism has been discussed. The potential applications of carbon nanotube arrays in flat panel display and in synthesizing of other semiconducting nanorods on silicon substrates through the carbon nanotube-confined reaction have been proved. The synthesis process should be completely compatible with existing semiconductor technology and thus allow large-scale integration of organized nanotubes and nanowires into silicon.

Acknowledgements

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